electrode is formed in direct contact over entire said top surface of said fourth semiconductor layer between said at least one first trench and said at least one second trench.

32. (New) The semiconductor device according to claim 1, wherein said first material is identical to said second material.

IN THE ABSTRACT

Page 41, lines 2-15, please amend the Abstract to read as follows:

A semiconductor device capable of minimizing an increase in a gate capacity without adversely influencing an operation characteristic and a method of manufacturing the semiconductor device. A first trench and a second trench are formed to reach an upper layer portion of an N^- layer through a P base layer and an N layer, respectively. A predetermined number of second trenches are formed between first trenches. The first trench is provided vicinal to an N^+ emitter region and has a gate electrode formed therein. The second trench has a polysilicon region formed therein. The second trench is different from the first trench in that the N^+ emitter region is not formed in a vicinal region of the second trench and the gate electrode is not formed therein. A trench space between the first trench and the second trench which are provided adjacently to each other is set to not reduce a breakdown voltage. An emitter electrode is directly formed on an almost whole surface of a base region.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-13 and 21-32 are pending in the present application. Claims 1-6, 8-11 and